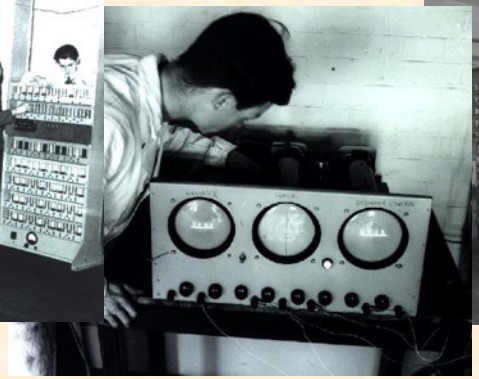
# Electronic Delay Storage Automatic Calculator

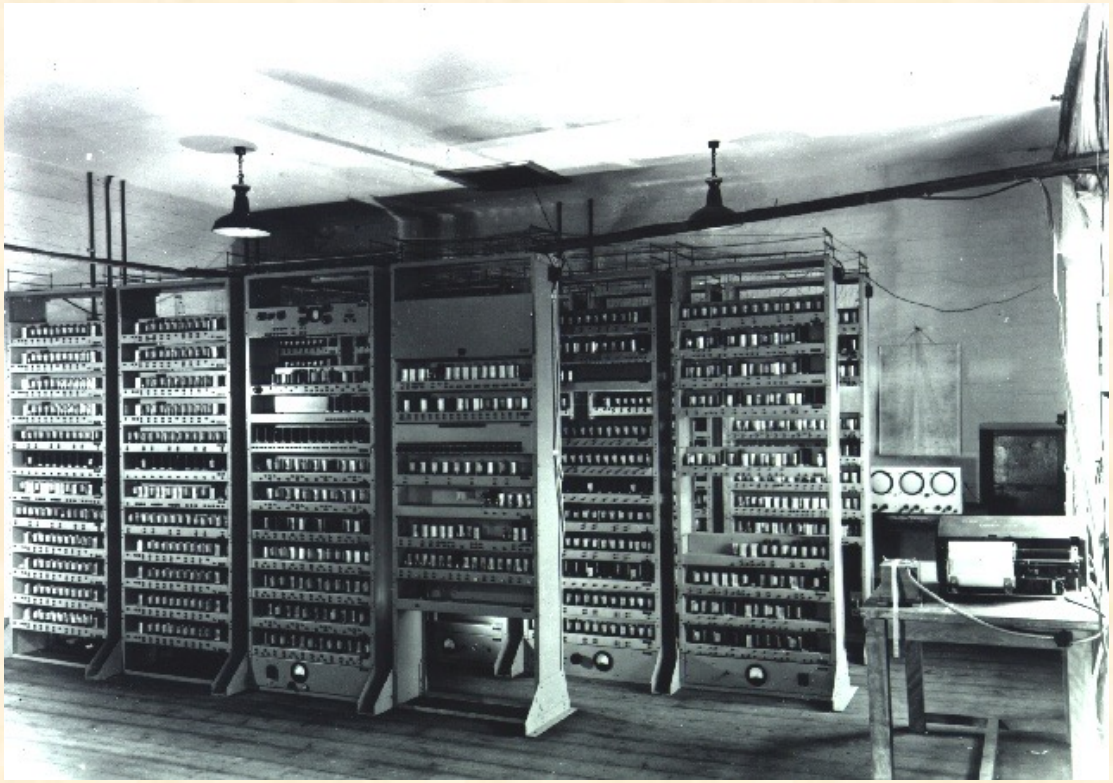



# Reconstructing EDSAC

## Andrew Herbert

## 25th April 2024

# The Project



Build a working reconstruction of Cambridge University's EDSAC Computer as it was when it provided the world's first computing service in 1950/51.

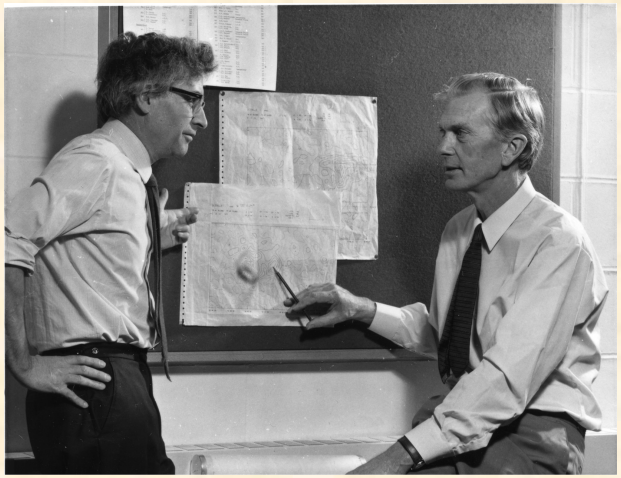
# Why Build a Replica of EDSAC?

- To celebrate an early triumph of British computer technology – and the creation of the world's first practical electronic stored program computer.
- To give us a better understanding of our computer heritage and create a new archive of historic material about early computing.
- To revive disappearing expertise and learn about the technical challenges faced by the early computer pioneers.
- A valuable new and living educational resource at The UK National Museum of Computing.

# EDSAC Achievements

1. The first *practical* **general purpose, stored program, electronic, digital computer.**
   - provided a *computing service* for the University of Cambridge.
2. The invention of **software**:
   - first machine to read in symbolic programs.
   - Extensive library of "subroutines".
3. Transformed science:
   - 1500 times faster than the mechanical calculators it replaced.
   - responsible for 3 Nobel Prizes

# EDSAC Nobel Prize Winners

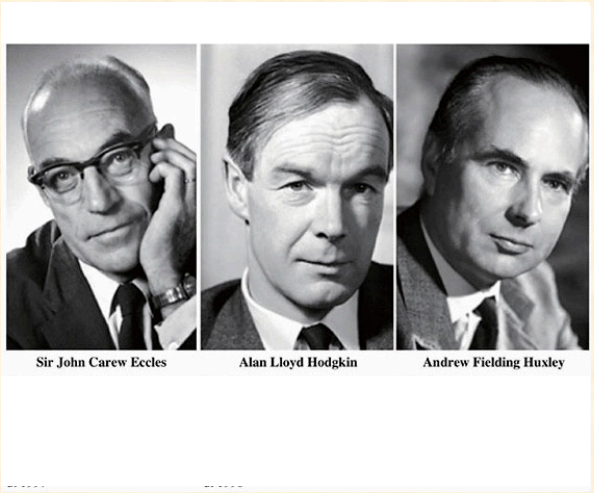


Martin Ryle & Anthony Hewish

Radio Astronomy

Photo: John T Scott,
Physics Today Collection

John Kendrew and Max Perutz
Structure of Globular Proteins
Photo: Medical Research Council




John Eccles,
Alan Hodgkin,
Andrew Huxley

Signalling in the Nervous System

Photo: Nobel Foundation

# Lyons and Computing

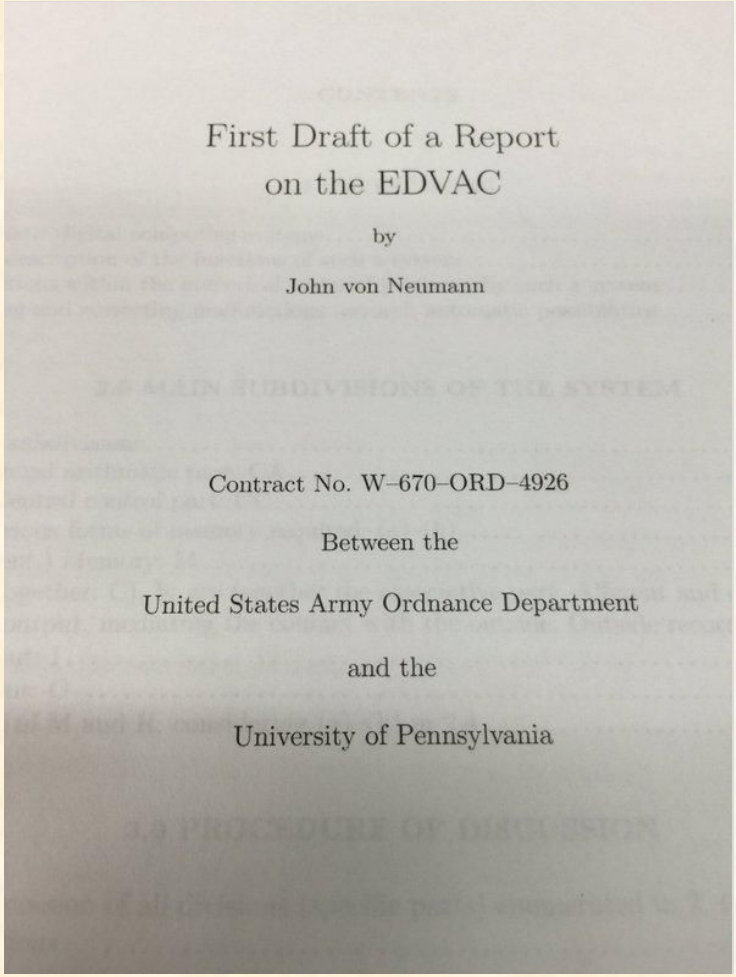
- Lyons interested in automatic information processing – low margins business + rising staff costs
- Von Neumann "First Draft of a Report on EDVAC" was circulating in UK in 1946/7 – people were thinking about "computers" and how they might be used
- Lyons executives visited USA to learn about computers
- Told to visit M.V. Wilkes at Cambridge University Mathematical Laboratory as EDSAC ahead of USA efforts

# EDSAC & LEO

- Prototype for LEO
- Improved engineering for greater reliability
- Added features for business computing
  - I/O
  - Decimal computation

- Pinkerton visited M.V. Wilkes at Cambridge Mathematical Laboratory to see EDSAC
- Ernest Lenaerts assigned to EDSAC Project
- Funds donated to Mathematical Laboratory to help project progress more rapidly

# The EDSAC Story



First Draft of a Report
on the EDVAC

by

John von Neumann

Contract No. W–670–ORD–4926

Between the

United States Army Ordnance Department

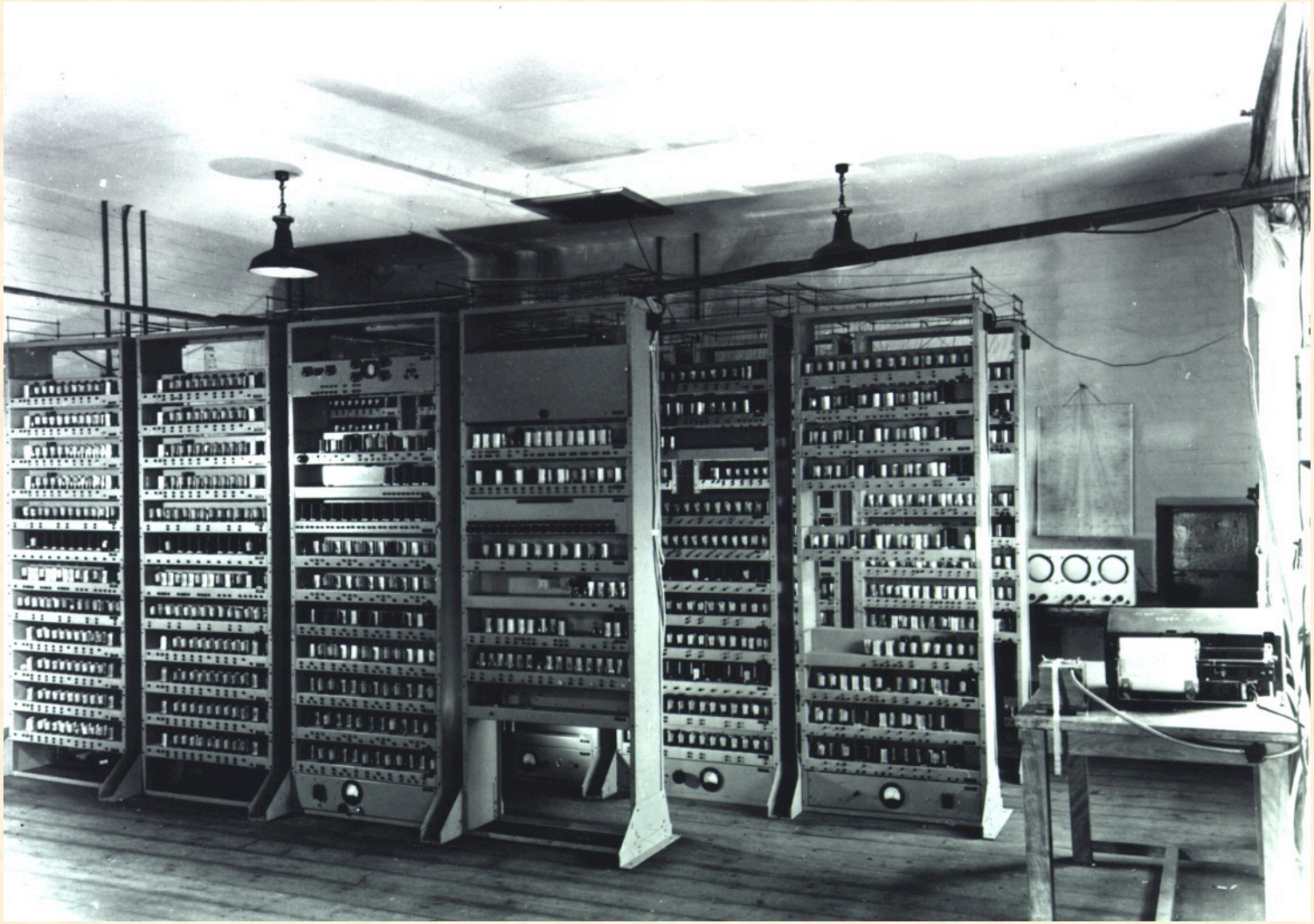
and the

University of Pennsylvania

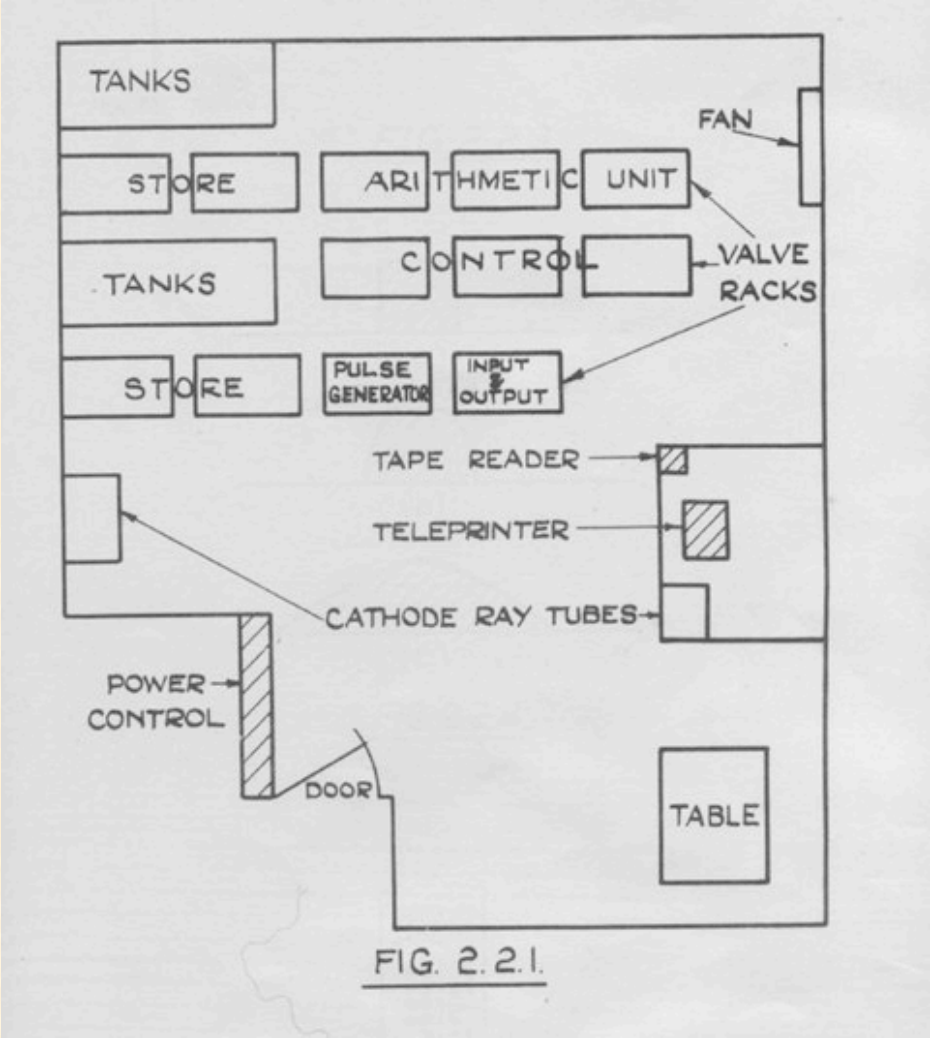
# M.V. Wilkes (1913-2010)

- B.A. Mathematics, St John's College, Cambridge
- PhD, Physics, Cavendish Laboratory
- War time radar expert
- Director of Cambridge Mathematical Laboratory
- John Von Neumann: "Draft Report on the EDVAC"
- Princeton Conference 1948

# EDSAC (1949)



# EDSAC




Dodd & Glennie ARE Report 7/51 1951

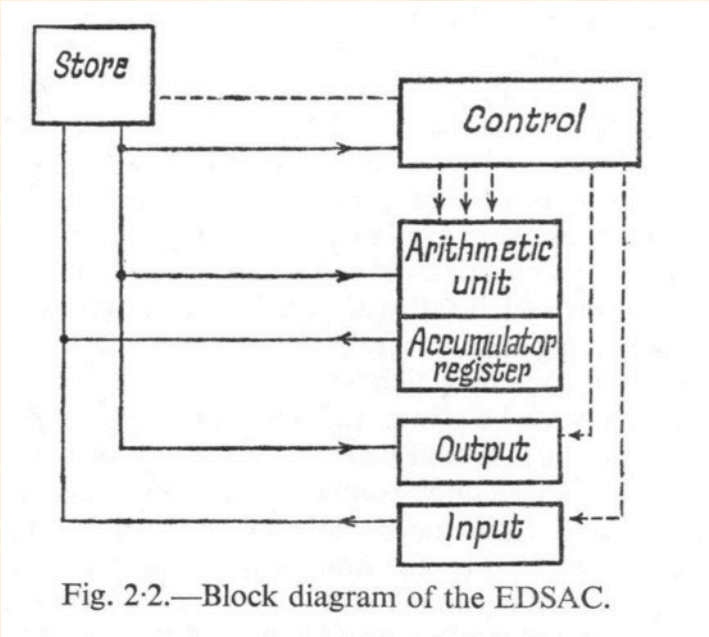



Fig. 2·2.—Block diagram of the EDSAC.

Automatic Digital Computers,
M.V. Wilkes, 1956

# EDSAC Architecture

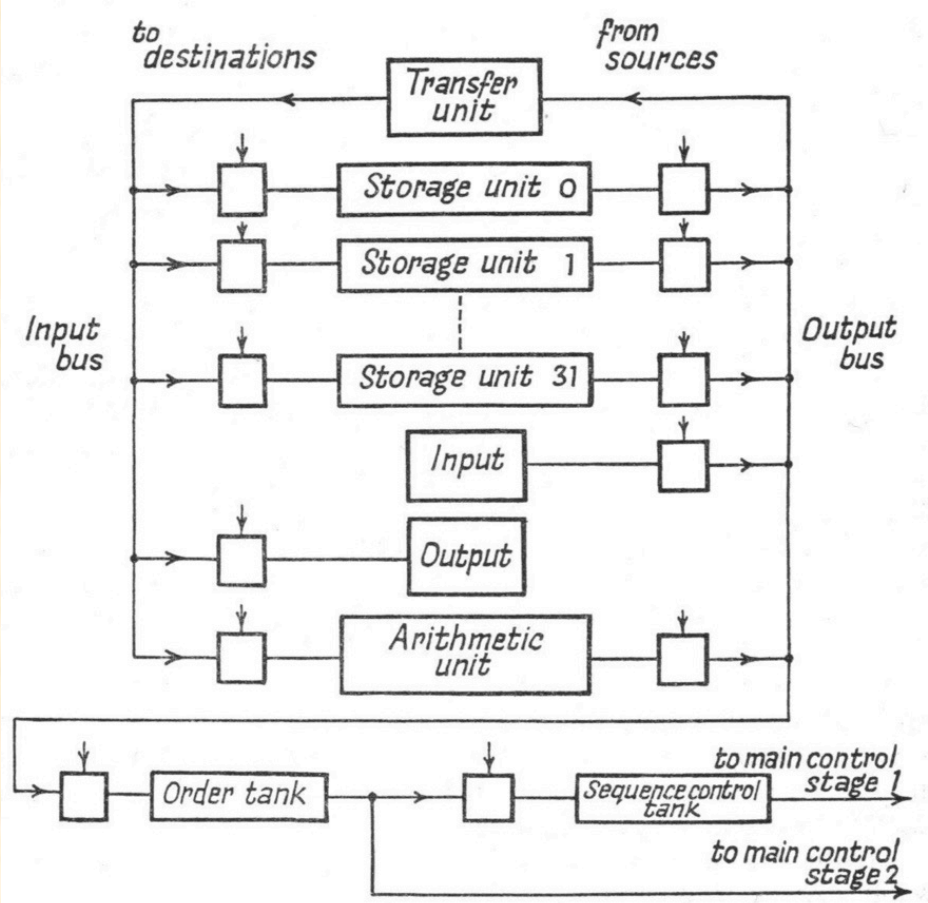



Fig. 2·3.—Numerical interconnexions in the EDSAC.

Automatic Digital Computers, M.V. Wilkes, 1956

# Computer Memory in 1949

- Too expensive to build an electronic memory.
  - 5 tubes per bit * 17 * 1024
    = 79,000 tubes.
- Acoustic delay lines.
- Williams (cathode ray) tubes.
- Rotating magnetic drums.
- All were complex, expensive and unreliable.
- All limited speed of the "computer".

# EDSAC Acoustic Delay Lines

Maurice Wilkes with a battery of 16 storage tanks, each holding 16 x 36 bit words.

The 5 ft steel tubes contain mercury as the acoustic delay medium.

Designed by T. Gold.

# Serial Computing

Most of EDSAC is serial
Process one bit of a word at the time
Reduces number of components needed

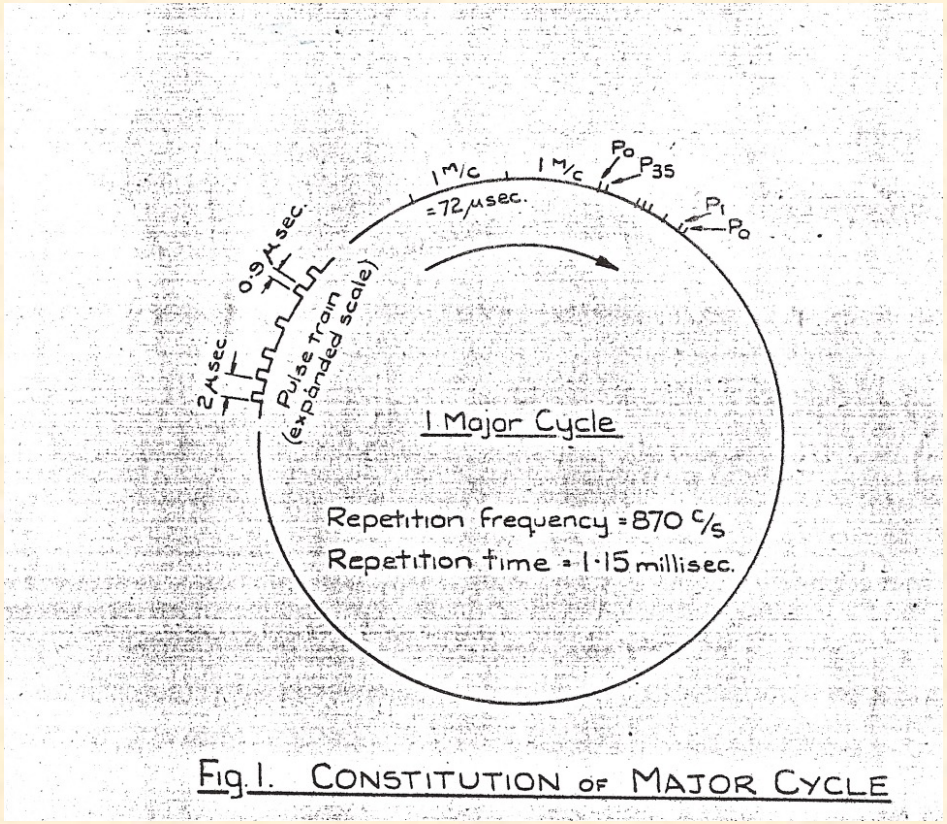


Fig. 1. Constitution of Major Cycle

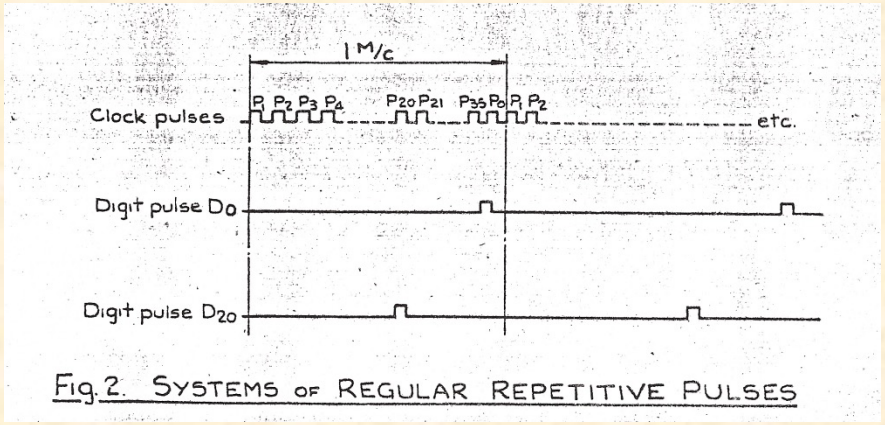


Fig. 2. Systems of Regular Repetitive Pulses

From Edsac Report

# Decoding and Coincidence

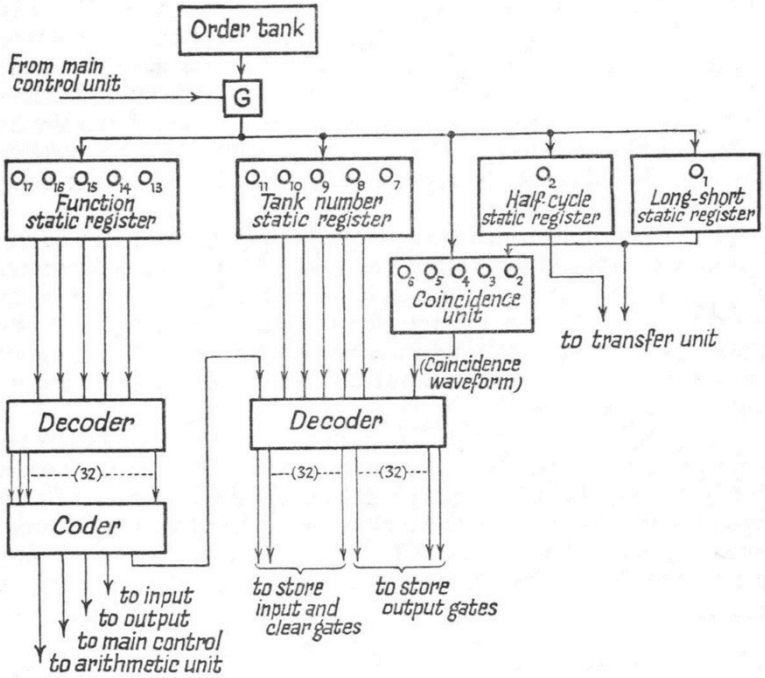
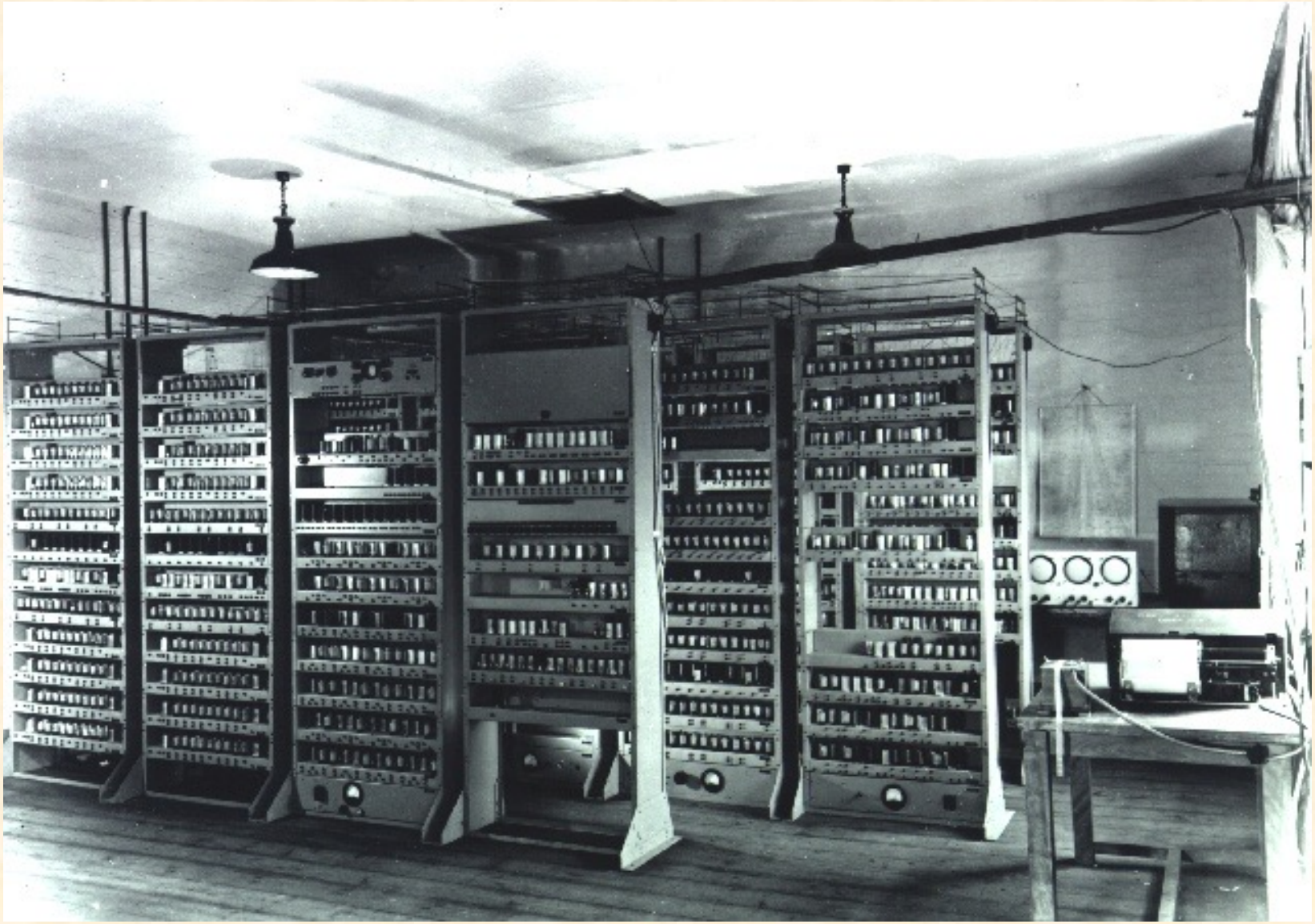



Fig. 2·4.—Block diagram showing how orders are interpreted in Stage II of the control sequence.

Have to go parallel to decode function number and memory address

Automatic Digital Computers, M.V. Wilkes, 1956

# Building the Replica



# Authenticity

We don't have a complete blueprint,
so we aim to...

- be consistent with photographs and contemporary records.
- use period components and circuits when available and suitable.
- Use functionally equivalent modern components otherwise.
- adhere to EDSAC "principles" when filling in gaps.

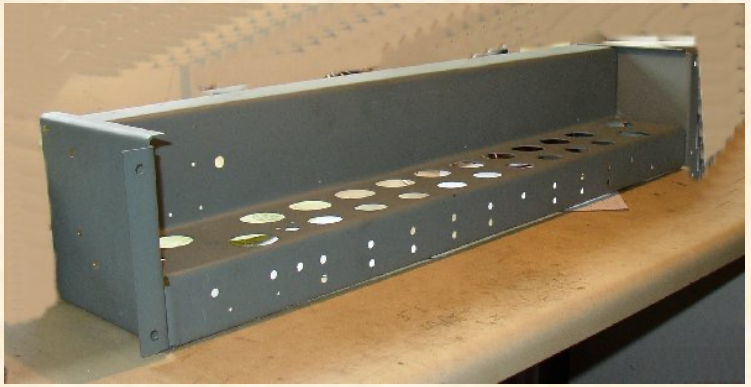
# Documents & Knowledge Acquisition

- Original (incomplete) technical description & logical design outline from Cambridge Computer Laboratory archives.
- Original photographs & published papers.
- Recollections of pioneers.
- Found cache of ~20 circuit diagrams for "the later EDSAC".
- EDSAC ran for 10 years so need to understand the evolution of the machine (our target: 1950/51).

# Mechanical Design

- Scanning and measuring from photos.
- 12 racks, 142 chassis ("panels").
- An original chassis exists to measure.

- Drawn up using CAD.
- At the outset we didn't know how many different types of chassis there were, or where they were placed in the racks.



# Rack and Chassis Manufacturing


Teversham Engineering, Cambridge

# Logic Design & Simulation

- Need to know how EDSAC works in detail
- Incomplete & inconsistent diagrams
- Evidence of much re-design during commissioning
- Need to extrapolate undocumented areas of logic
- Simulation essential to give confidence before committing to building anything

# Typical Logical Diagram

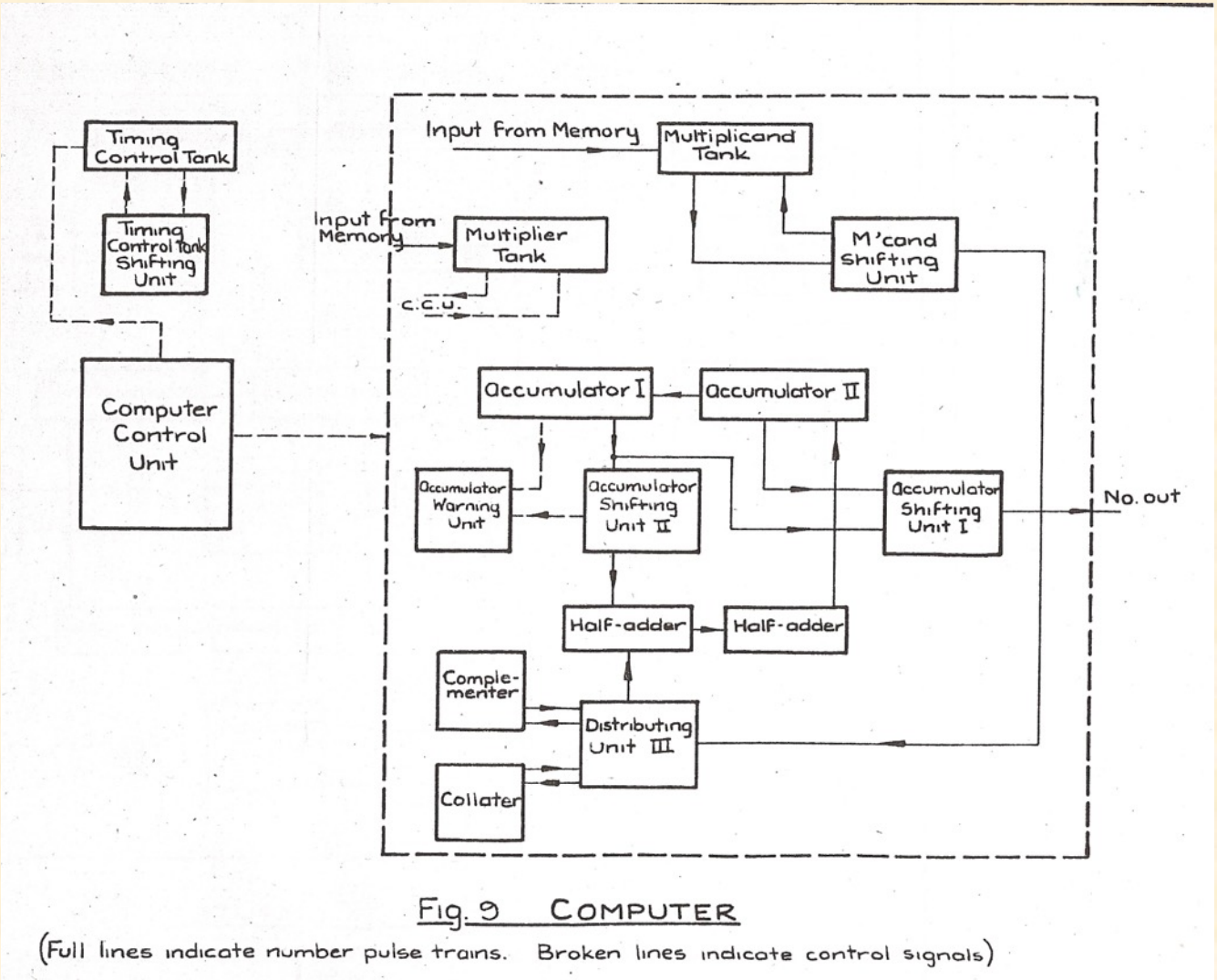



Fig. 9 COMPUTER

(Full lines indicate number pulse trains. Broken lines indicate control signals)

From EDSAC Report

# Typical Timing Diagram

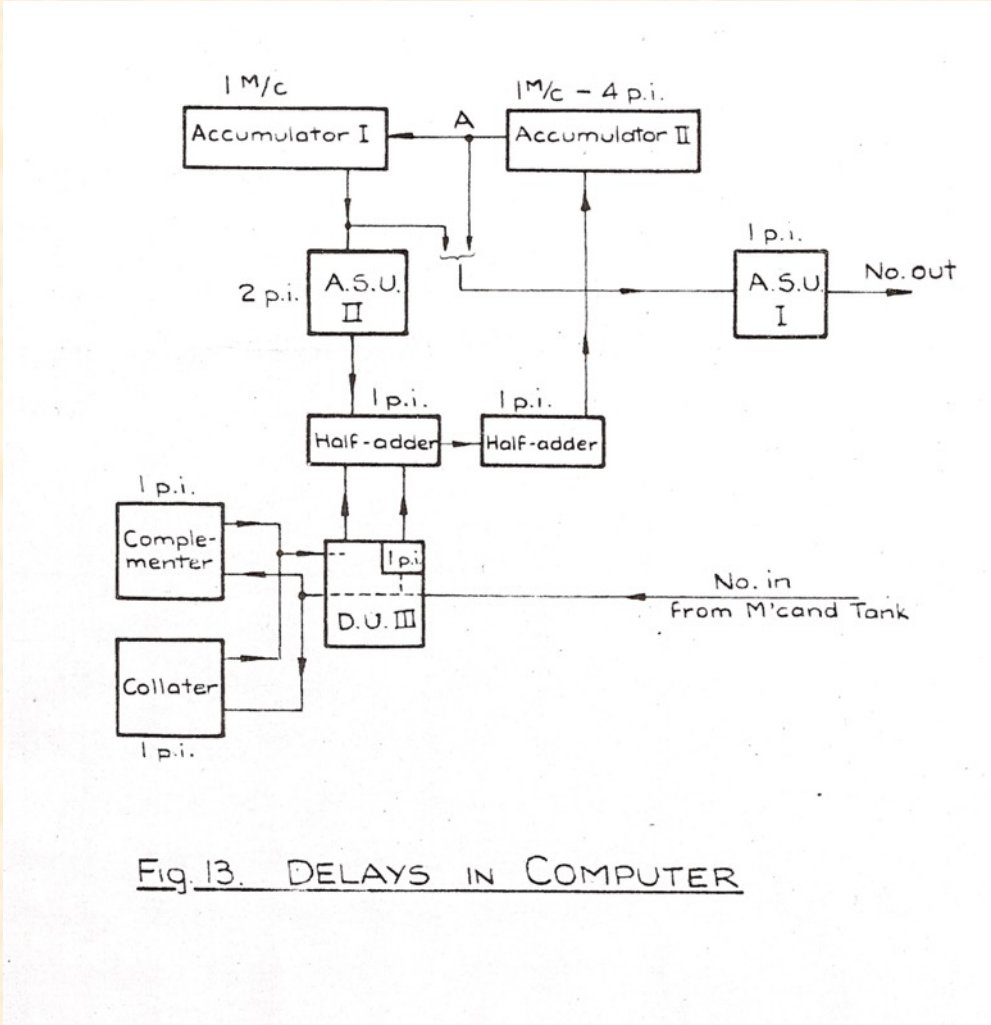
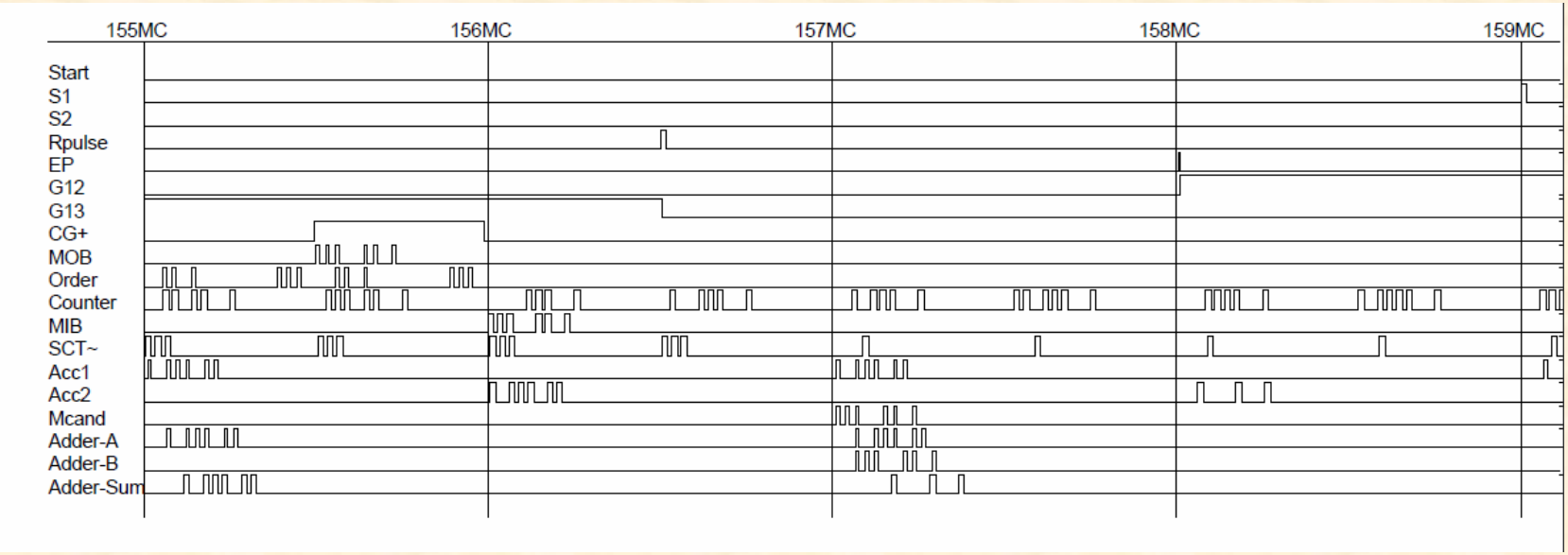



Fig. 13. DELAYS IN COMPUTER

From EDSAC Report

# Logic Simulation

- Bill Purvis wrote a simulator for whole logic - can run a program, very slowly.
- Now translated to Verilog and running on an FPGA.



# Electronic design

- EDSAC was built by radio and radar engineers with no knowledge of "digital logic" as we understand it today.
- "Computing with waveforms", F.C. Williams
- Common circuit elements aid identification: flip-flop, inverter, short delay, pulse amplifier.
- Lots of circuit simplification to reduce valve count and stage delays but introduces problems with noise.
- System requires careful tuning to ensure signals arrive "on time".

# Typical Circuit Diagram

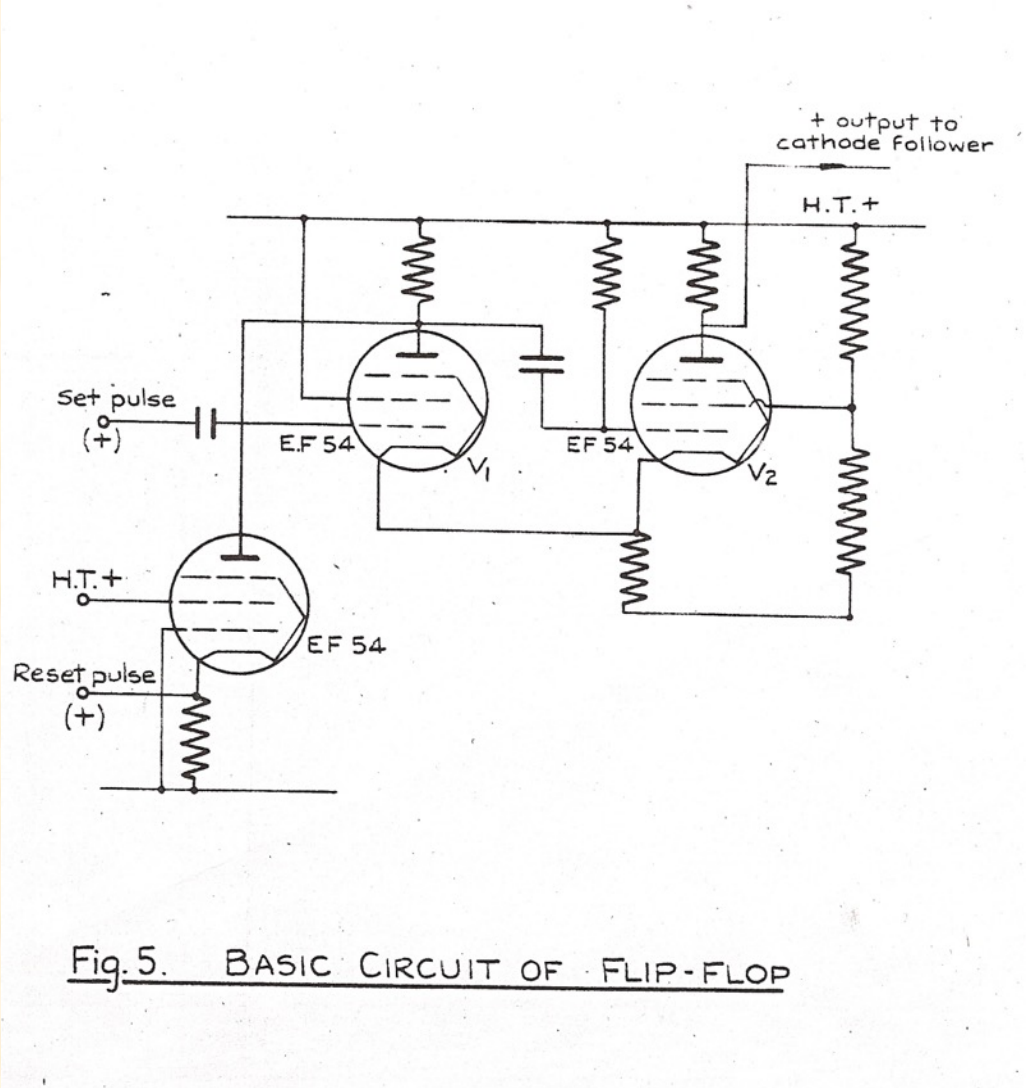
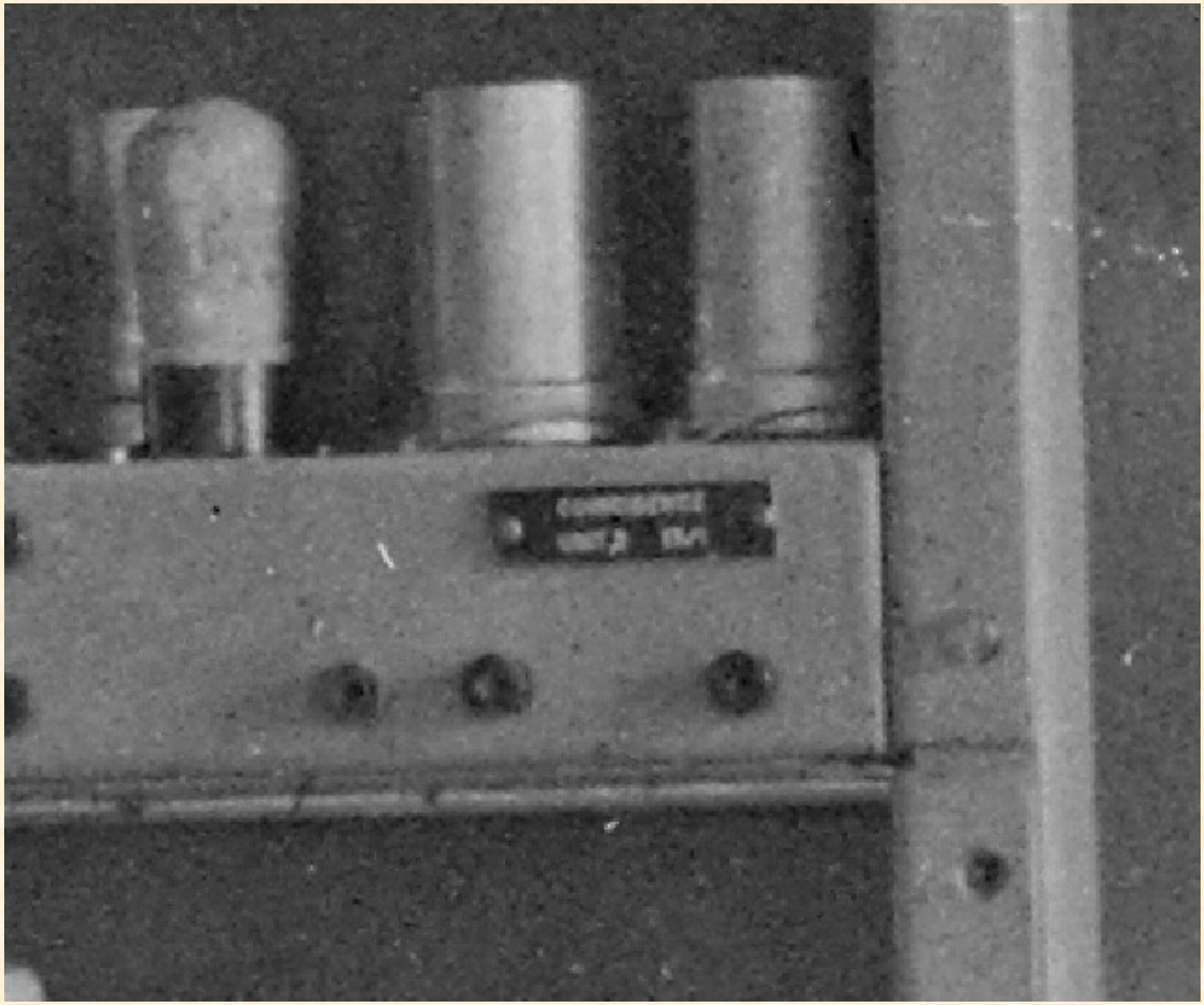


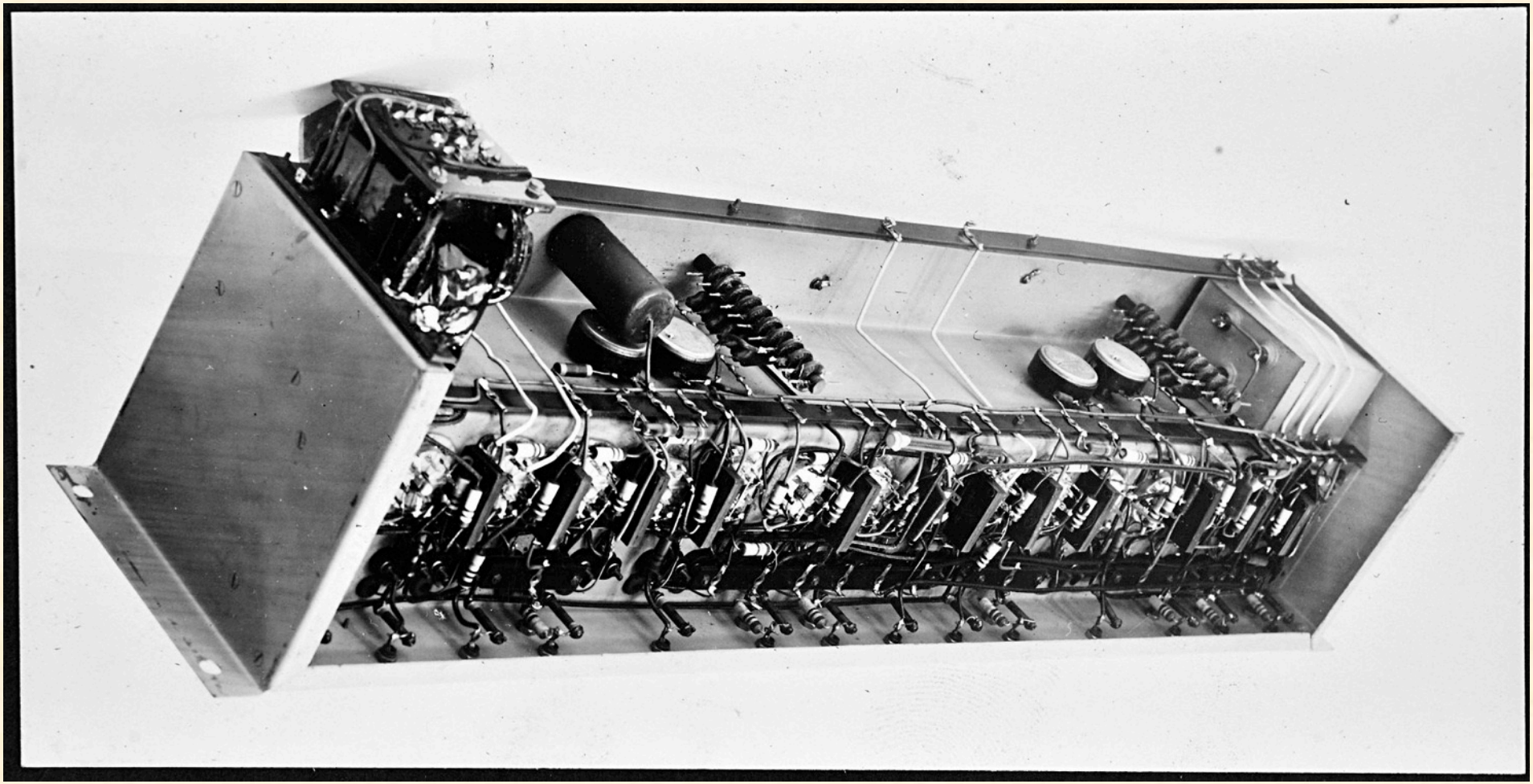

Fig. 5. BASIC CIRCUIT OF FLIP-FLOP

From EDSAC Report

# Mapping Logic to Chassis

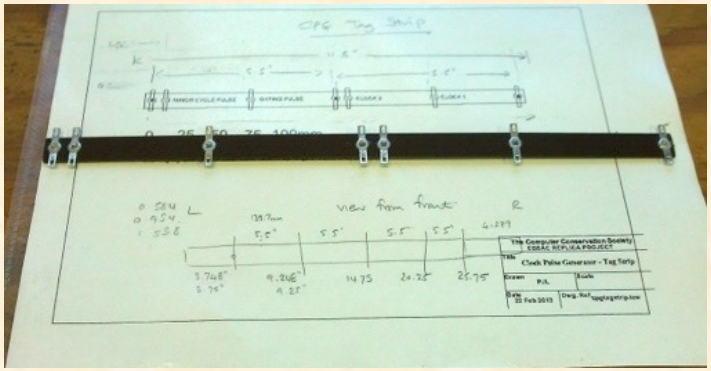


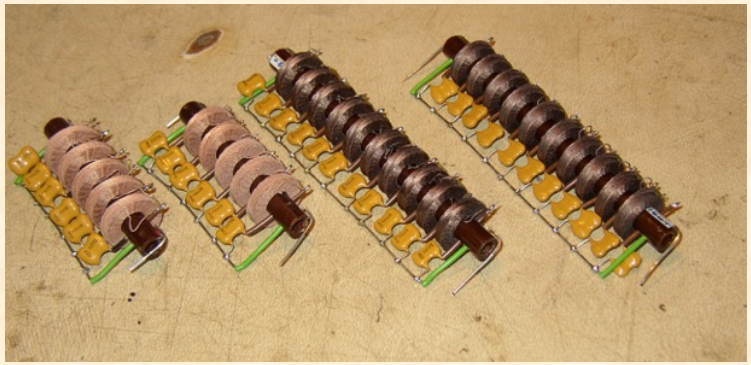
# 1949 Chassis



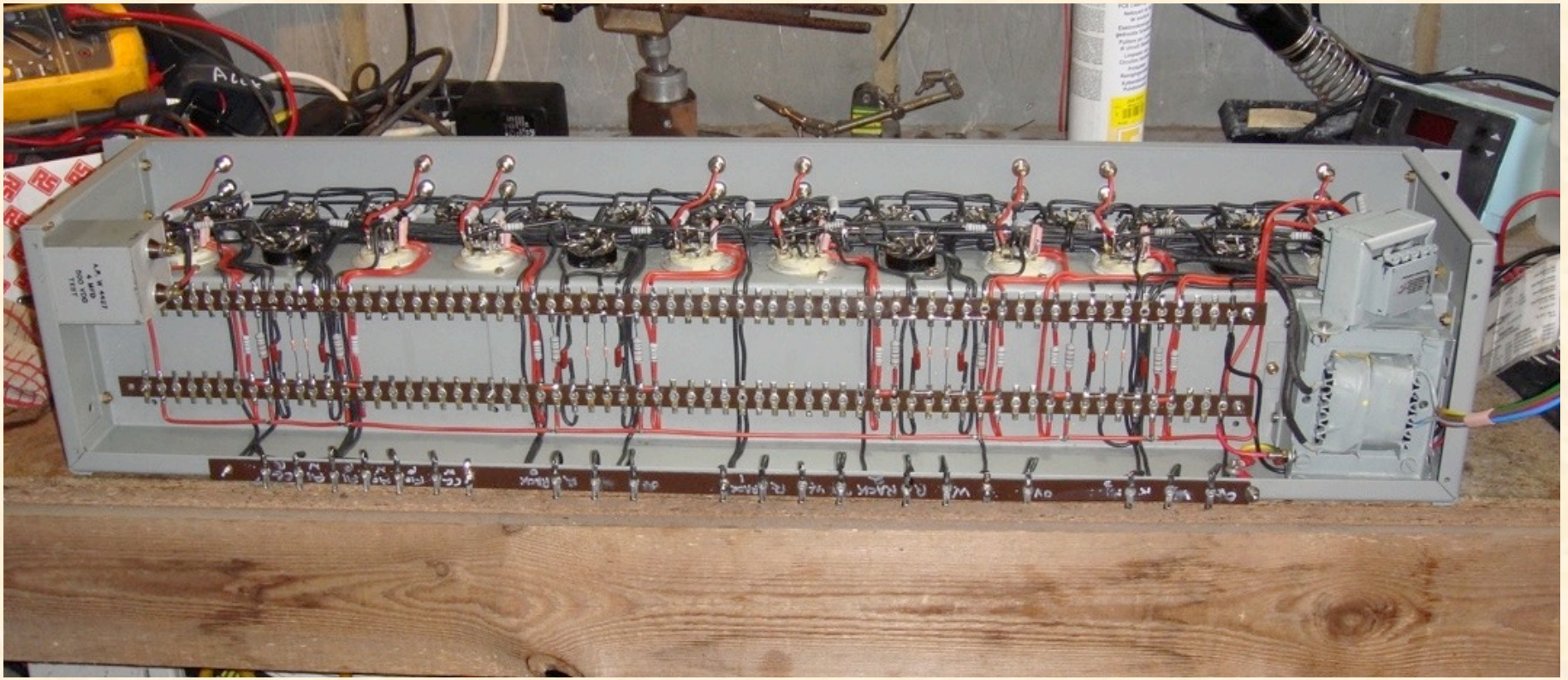
# Acquisition of Parts

- Many, but not all, thermionic valves are available commercially as "new old stock".
- B9G valve holders are problematic.
- Authentic 'period' resistors and capacitors are too unreliable to use.
- Hand made tag strips and coils.





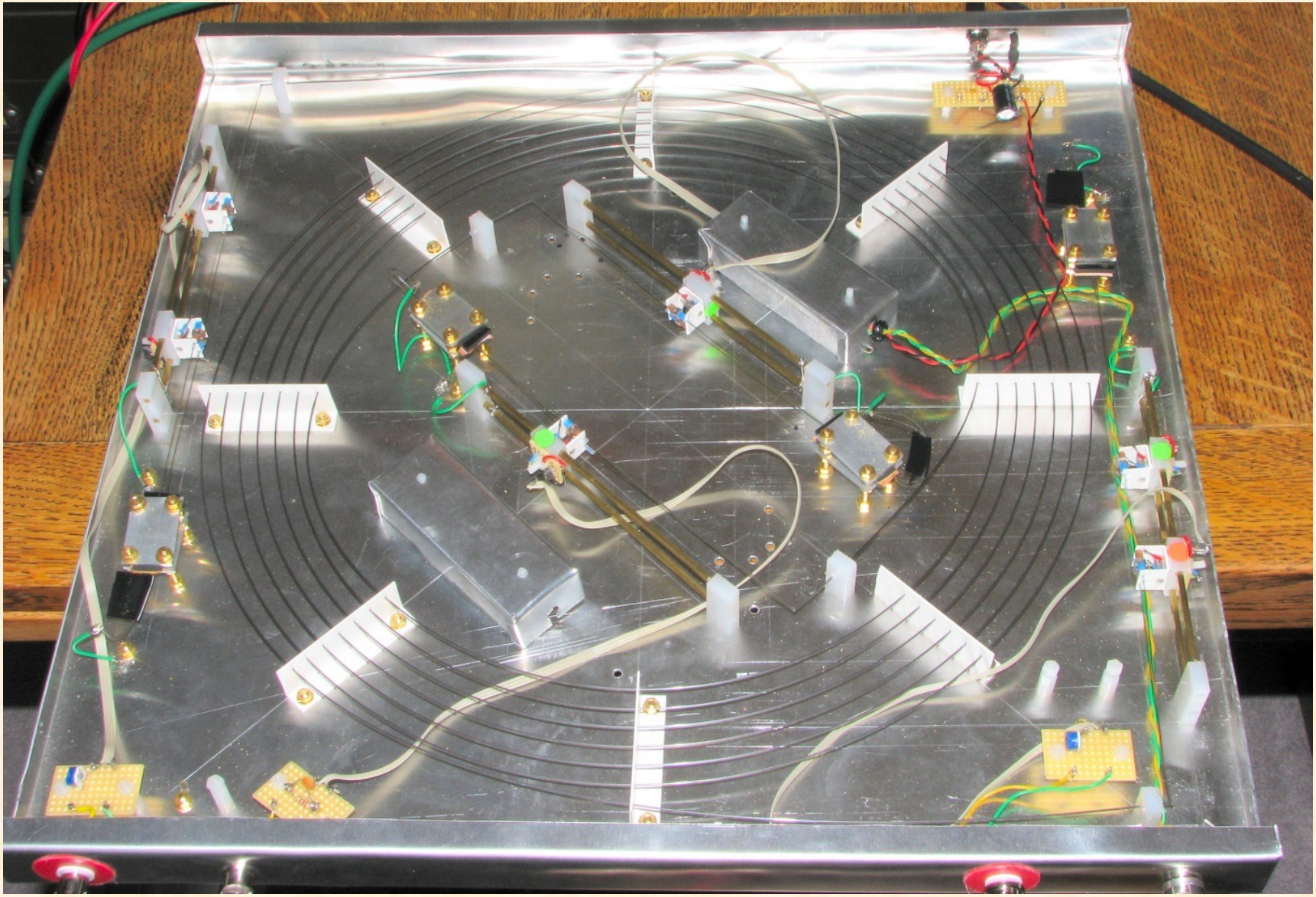
# Replica Chassis



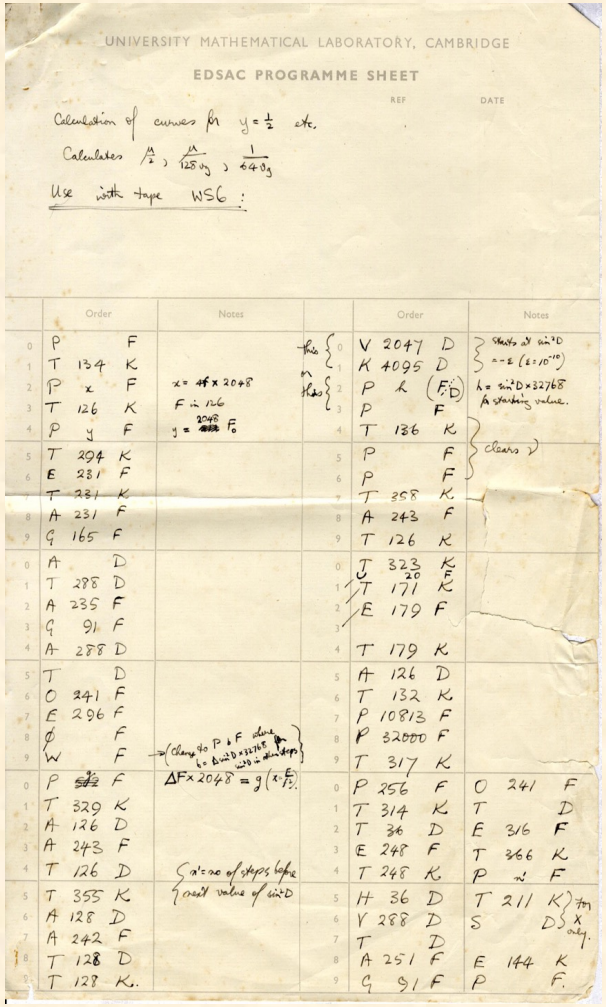
# Replica Memory Tanks

- Risky and costly to use mercury, except perhaps in one example tank.
- Temperature stability is a major issue.
- Precision engineering required: tubes and end plates – aligned to within 0.001" end-to-end.
- Using magnetostrictive nickel delay lines as a reasonable alternative.
- Use semiconductor shift registers to get off the ground quickly.

# Short Nickel Delay Line



# Programming EDSAC



UNIVERSITY MATHEMATICAL LABORATORY, CAMBRIDGE

EDSAC PROGRAMME SHEET

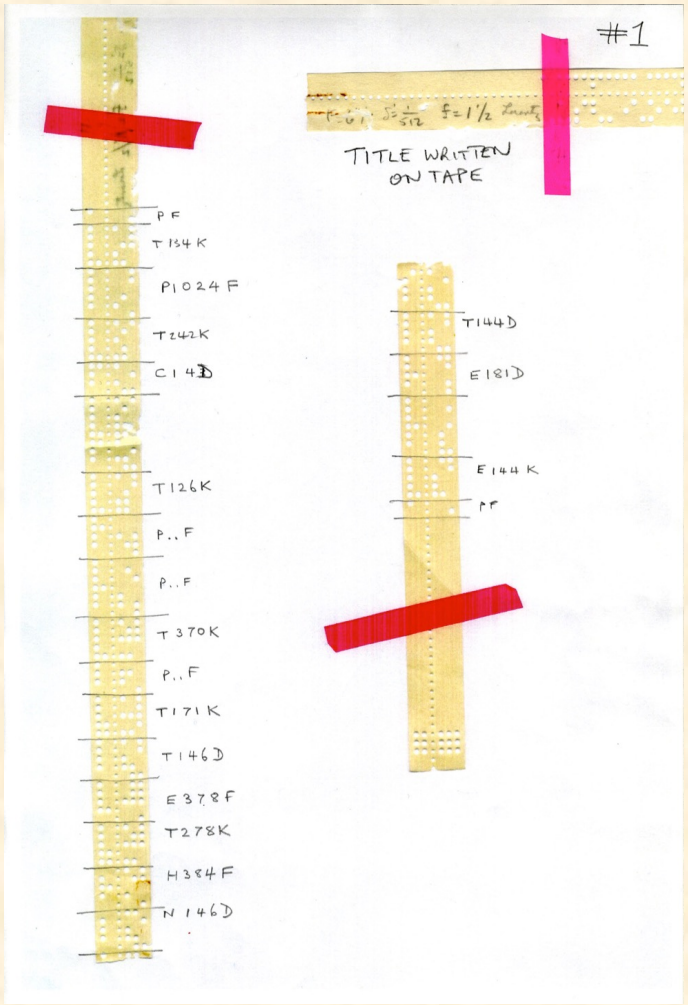
REF DATE

Calculation of curves for $y = \frac{1}{2}$ etc.

Calculates $\frac{M}{2}$, $\frac{M}{125 v_0}$, $\frac{1}{640 v_0}$

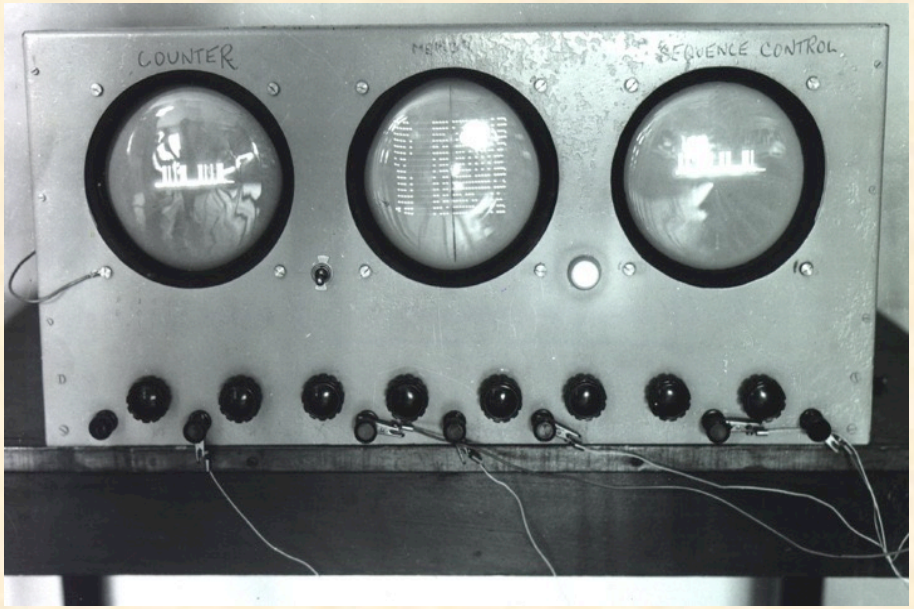
Use with tape WS6 :

| | Order | | Notes | | Order | | Notes |
|---|---|---|---|---|---|---|---|
| 0 | P | F | | this | V 2047 | D | starts at $\sin^2 D = -2 (\varepsilon = 10^{-10})$ |
| 1 | T 134 | K | | | K 4095 | D | |
| 2 | P x | F | $x = 4f \times 2048$ | | P h | (F D) | $h = \sin^2 D \times 32768$ |
| 3 | T 126 | K | $F$ in 126 | | P | F | $h$ starting value. |
| 4 | P y | F | $y = \frac{2048}{} F_0$ | | T 136 | K | |
| 5 | T 294 | K | | | P | F | clears |
| 6 | E 281 | F | | | P | F | |
| 7 | T 281 | K | | | T 358 | K | |
| 8 | A 231 | F | | | A 243 | F | |
| 9 | G 165 | F | | | T 126 | K | |
| 0 | A | D | | | T 323 | K | |
| 1 | T 288 | D | | | U 20 F | | |
| 2 | A 235 | F | | | T 171 | K | |
| 3 | G 91 | F | | | E 179 | F | |
| 4 | A 288 | D | | | T 179 | K | |
| 5 | T | D | | | A 126 | D | |
| 6 | O 241 | F | | | T 132 | K | |
| 7 | E 296 | F | | | P 10813 | F | |
| 8 | Ø | F | change to P & F above | | P 32000 | F | |
| 9 | W | F | $h = \sin^2 D \times 32768$ with $D$ in alternate steps | | T 317 | K | |
| 0 | P | F | $\Delta F \times 2048 = g(x \frac{F}{P})$ | | P 256 | F | O 241 F |
| 1 | T 329 | K | | | T 314 | K | T D |
| 2 | A 126 | D | | | T 36 | D | E 316 F |
| 3 | A 243 | F | | | E 248 | F | T 366 K |
| 4 | T 126 | D | $x$ = no of steps before exact value of $\sin^2 D$ | | T 248 | K | P F |
| 5 | T 355 | K | | | H 36 | D | T 211 K) for |
| 6 | A 128 | D | | | V 288 | D | S D) X only. |
| 7 | A 242 | F | | | T | D | |
| 8 | T 128 | D | | | A 251 | F | E 144 K |
| 9 | T 128 | K. | | | G 91 | F | P F. |

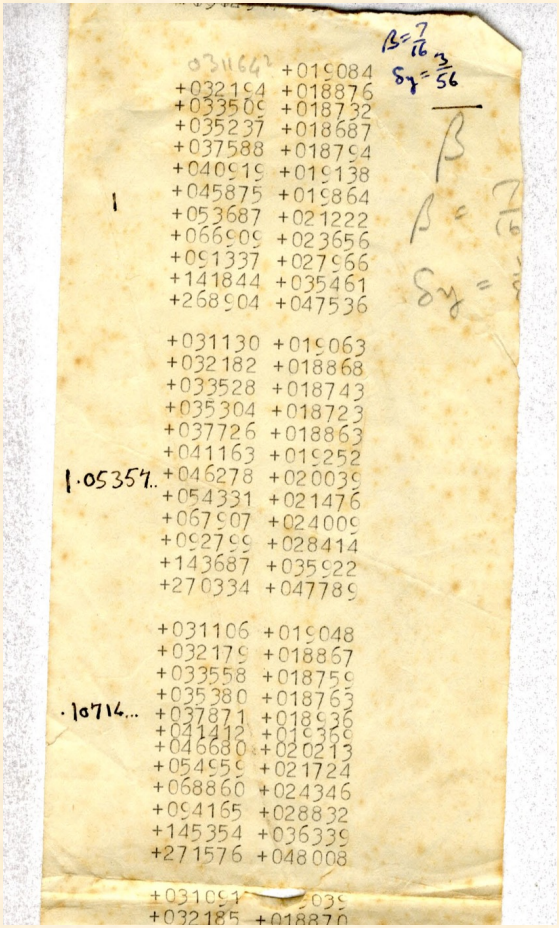


# Program Preparation

# Operating EDSAC



# Output


β=7/16
δγ=3/56
β
β = 7/16
δγ =
034642 +019084
+032194 +018876
+033509 +018732
+035237 +018687
+037588 +018754
+040919 +019138
+045875 +019864
+053687 +021222
+066909 +023656
+091337 +027966
+141844 +035461
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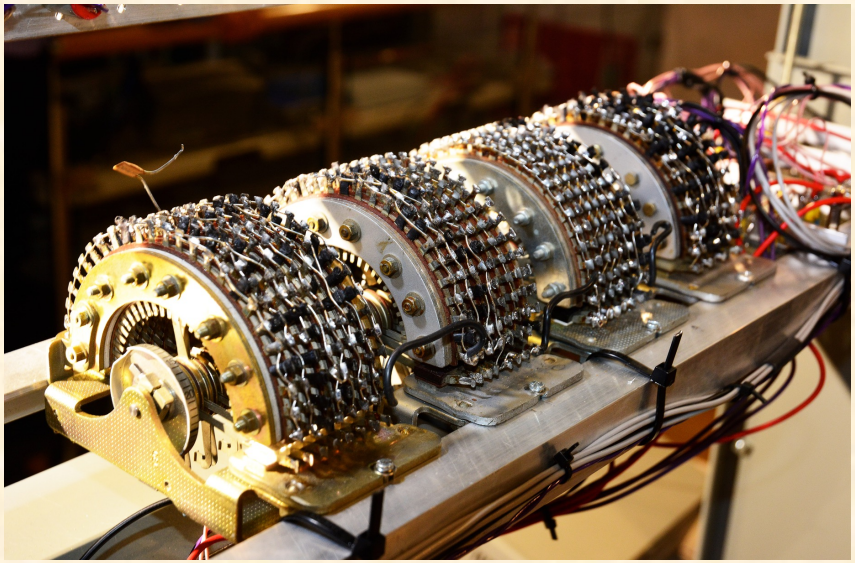
+032185 +018870

# Initial Orders



- Loaded on "START"
- Reads in user program
- Combined "assembler" and "linker"
- Extensive library of subroutines – input, output, mathematical functions
- Alphanumeric source code
- Parametric addressing to allow position independent code

# Status (March 2024)

- 140 chassis built and tested of 142 total.
- Clock and Digit Pulse system working.
- Memory recirculation, addressing and coincidence working.
- Main control working.
- Transfer unit working.
- Delay line register stores working.
- Main store delay lines in commissioning.
- Systematic testing of arithmetic functions underway
- I/O and Initial Orders under construction

# To Find Out More

- Visit www.edsac.org web site
- Download EDSAC simulator from http://www.dcs.warwick.ac.uk/~edsac/